## Claims

What is claimed is:

1. A memory controller comprising a compression map cache, said compression map cache to store information that identifies a cache line's worth of information that has been compressed with another cache line's worth of information.

2. A processor and a memory controller integrated on a same semiconductor die, said memory controller comprising a compression map cache, said compression map cache to store information that identifies a cache line's worth of information that has been compressed with another cache line's worth of information.